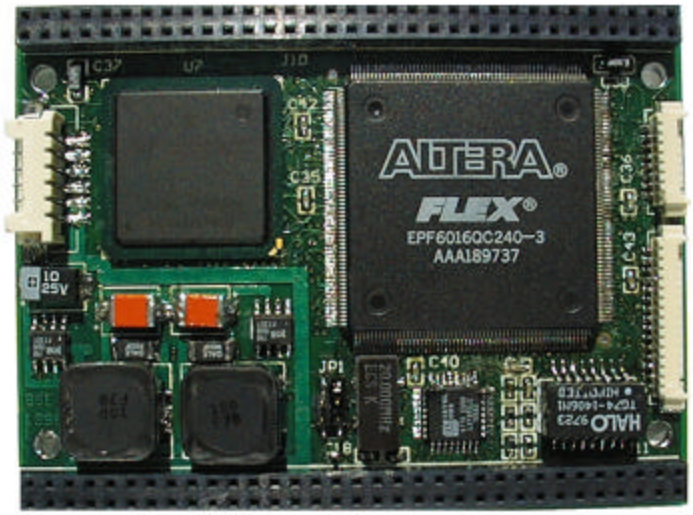
ipEngine-1



(Actual Size)

66 MIPS Power PC CPU

16 MB DRAM

2 MB FLASH

10Base-T Ethernet

On-Board Power Supply

16,000 Gate FPGA

132 Pin Virtual I/O Interface

USB Host/Slave Controller

LCD/Video Controller

Dual RS-232

Built-In Real-Time Network OS and Web Server

Integrated Development Tools

The Internet revolution that has swept the desktop computing world is rapidly making its way into the embedded marketplace. OEMs not currently in the networking market, however, are finding that the cost of "internet enabling" their products can be prohibitive in terms of both time-to-market delays as well as significant startup and long-term maintenance costs.

Bright Star Engineering's *ipEngine* promises to significantly reduce these entry costs by providing a vertically integrated "network engine" complete with the hardware, software, and development environment required to internet-enable a product. By employing POSIX and ANSI C standards, the *ipEngine*'s software environment leverages a familiar programming environment and facilitates migration of software from UNIX and Windows 95/NT platforms.

The *ipEngine* utilizes Motorola's PowerPC™ MPC823 processor with an array of on-chip peripherals including Ethernet, USB, LCD/Video, I_2C and serial controllers. The on-board flash memory file system provides storage for the operating system as well as OEM application software and data.

The external interface to the *ipEngine* hardware is via an FPGA-based 88 pin "virtual interface" which can be configured on the fly to adapt to the OEM's needs. The FPGA can be configured to emulate a variety of bus architectures as well as to implement peripheral functions like UARTs, PWM control, memory emulation, data capture and synthesis, and interfaces to a variety of input devices.

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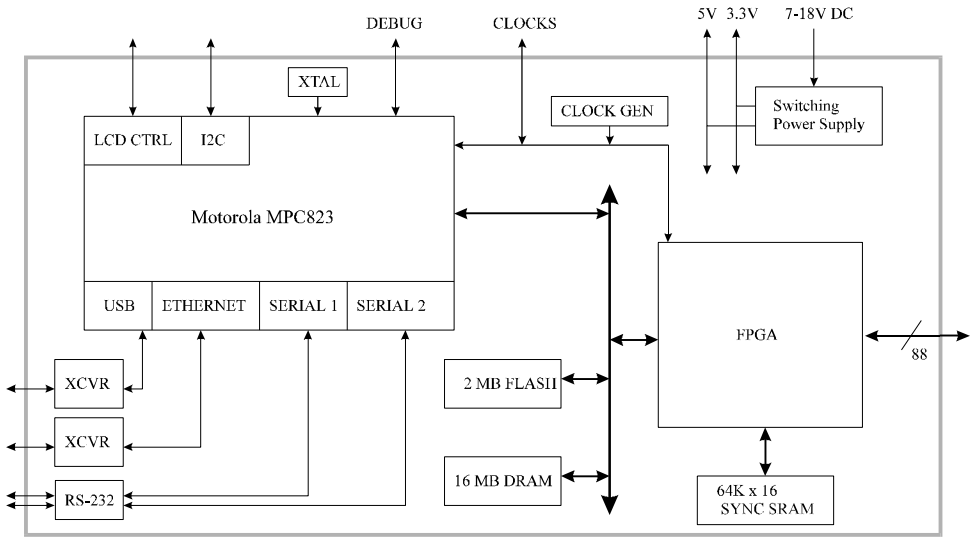
ipEngine Block Diagram



Specifications

CPU

- Motorola MPC823 @ 0-50 MHz
  On-Chip Peripherals:
  - Ethernet
  - USB Host/Slave
  - 2 Serial Channels
  - LCD/Video Controller
  - I_2C Serial Bus

Memory

- 4Mx32 60ns EDO DRAM
- 1Mx16 90ns BootBlock FLASH

FPGA Based Virtual I/O Interface

- Altera EPF6016 16,000 Gate FPGA
- 64K x 16 Sync SRAM
- 1 – 50 MHz Programmable Clock Generator
- 88 Pins "Virtual I/O"

Power Supply

- Input: 7-18V unregulated DC
  or regulated 5V DC
- Output: 5.0V @ 2 amps (with 7-18V input)
  3.3V @ 2 amps
- Efficiency: 95%

Power Consumption

- 25mW – 2 Watts depending on application

Integrated Real-Time OS

- POSIX-based Kernel
- POSIX Threads
- Full-Complement of Network Protocols:
  - TCP/IP, UDP, ICMP, ARP, IGMP, DNS
  - FTP, TFTP, HTTP, DHCP
  - TELNET
  - Berkeley Sockets
- Command Line Shell
- Embedded Apache Web Server
- URL/Web based File System
- Remote "Over-the-Network" Debugging
- Boot Loader for support of third-party RTOS

Integrated Development Tools

- GNU based C/C++ Cross-Development
- No-Cost FPGA Tools available from Altera Web Site

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